CLAIMS:

1. A packet formatter (240) for use in a television receiver (200) capable of receiving a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream, said packet formatter (240) comprising:

a first processing block (410) capable of receiving said dual bitstream signal and removing therefrom header bits and parity bits associated with said robust stream to thereby produce a first output signal; and

a second processing block (430) capable of receiving said first output signal and removing therefrom duplicate bits associated with said robust stream to thereby produce a second output signal that is output from a data path output (295) of said packet formatter (240).

2. The packet formatter (240) as set forth in Claim 1 wherein said packet formatter (240) passes bytes associated with said standard stream to said data path output (295) of said packet formatter (240) after delaying said standard stream bytes by a predetermined delay time.

3. The packet formatter (240) as set forth in Claim 2 wherein said packet formatter (240) comprises a third processing block (420) capable of determining the locations of said parity bits in said robust stream.

4. The packet formatter (240) as set forth in Claim 3 wherein said third processing block (420) is further capable of determining the locations of said header bits in said robust stream.

5. The packet formatter (240) as set forth in Claim 4 wherein said third processing block (420) comprises a look-up table (420).

6. The packet formatter (240) as set forth in Claim 5 wherein said packet formatter (240) generates and outputs packet identification information used by subsequent processing blocks (250, 260, 270) following said packet formatter (240).

7. A signal comprising the second output signal output from the data path output of the packet formatter (240) as set forth in Claim 1.

8. For use in a television receiver (200) capable of receiving a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream, a method of formatting packets of said dual bitstream signal comprising the steps of:

receiving in a packet formatter (240) said dual bitstream signal and removing therefrom header bits and parity bits associated with said robust stream to thereby produce a first output signal; and

removing from said first output signal duplicate bits associated with said robust stream to thereby produce a second output signal that is output from a data path output (295) of said packet formatter (240).

9. The method as set forth in Claim 8 further comprising the step of delaying bytes associated with said standard stream by a predetermined delay time before outputting said delayed standard stream bytes on said data path output (295) of said packet formatter (240).

10. The method as set forth in Claim 9 further comprising the step of determining the locations of said parity bits in said robust stream.

11. The method as set forth in Claim 10 further comprising the step of determining the locations of header bits in said robust stream.

12. The method as set forth in Claim 11 wherein said step of determining the locations of said parity bits comprises the step of determining the locations of said parity bits from a look-up table (420).

13. The method as set forth in Claim 12 further comprising the steps of generating and outputting packet identification information used by subsequent processing blocks (250, 260, 270) following said packet formatter (240).

14. A signal comprising the second output signal output from the data path output of the packet formatter (240) as set forth in Claim 8.

15. A television receiver (200) comprising:

receiver front-end circuitry capable of receiving and down-converting a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream to thereby produce a baseband signal; and

a forward error correction section capable of receiving said baseband signal from said receiver front-end circuitry, said forward error correction section comprising a packet formatter (240) comprising:

a first processing block (410) capable of receiving said standard stream and said robust stream associated with said baseband signal and removing therefrom header bits and parity bits associated with said robust stream to thereby produce a first output signal; and

a second processing block (430) capable of receiving said first output signal and removing therefrom duplicate bits associated with said robust stream to thereby produce a

second output signal that is output from a data path output (295) of said packet formatter (240).

16. The television receiver (200) as set forth in Claim 15 wherein said packet formatter (240) passes bytes associated with said standard stream to said data path output (295) of said packet formatter (240) after delaying said standard stream bytes by a predetermined delay time.

17. The television receiver (200) as set forth in Claim 16 wherein said packet formatter (240) comprises a third processing block (420) capable of determining the locations of said parity bits in said robust stream.

18. The television receiver (200) as set forth in Claim 17 wherein said third processing block (420) is further capable of determining the locations of said header bits in said robust stream.

19. The television receiver (200) as set forth in Claim 18 wherein said third processing block (420) comprises a look-up table (420).

20. The television receiver (200) as set forth in Claim 19 wherein said packet formatter (240) generates and outputs packet identification information used by subsequent processing blocks (250, 260, 270) following said packet formatter (240).

21. A data de-randomizer (270) for use in a television receiver (200) capable of receiving a dual bitstream signal comprising a standard stream compatible with the Advanced Television Systems Committee (ATSC) standard and a robust stream, said data de-randomizer (270) comprising:

a standard de-randomizer (710) capable of de-randomizing bytes associated with said standard stream; and

a robust de-randomizer (720) capable of de-randomizing bytes associated with said robust stream.

22. The data de-randomizer (270) as set forth in Claim 21 wherein said data de-randomizer (270) further comprises a delay calculation circuit (740, 750) for determining a delay with respect to a field synchronization signal associated with the robust stream.